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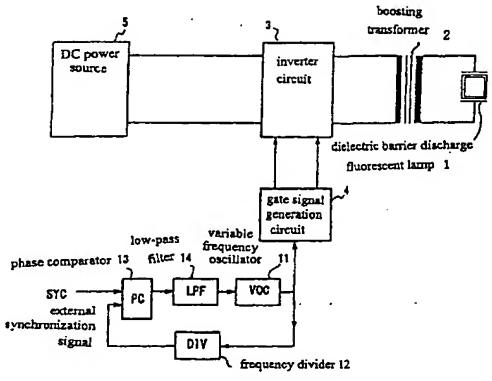
(54) LIGHT SOURCE

(57) This is an ideal light source device for use in image readout devices capable of light emission in which a dielectric barrier discharge fluorescent lamp is synchronized with an external synchronization signal without attendant fluctuation in optical power. Phase comparator (13) compares the oscillation signal phase of variable frequency oscillator (11) divided by frequency divider (12) with external synchronization signal (Sync), and controls the oscillation frequency of variable frequency oscillator (11) as a function of the phase difference. By so doing, the oscillation phase of variable frequency oscillator (11) is phase locked by external synchronization signal (Sync). The oscillation signal of variable frequency oscillator (11) is input to gate signal generation circuit (5), and the switch devices of inverter circuit (3) are opened and closed by the output of gate signal generation circuit (5). The direct current voltage output by DC power source (5)is converted into alternating current voltage. Alternating current voltage that is output by inverter circuit (3) is applied to lamp (1) via boosting transformer 2 to light lamp (1).

FIG. 1

Diagram showing the overall structure of a light source device in a first working example of the present invention.



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Description

Technical Field

[0001] The present invention concerns a light source device using a dielectric barrier discharge fluorescent lamp that fires utilizing ultraviolet light generated by dielectric barrier discharge.

Background Technology

[0002] Light source devices including dielectric barrier discharge fluorescent lamps are used as light sources of image readout devices.

[0003] Figure 10 is a diagram showing a constituent example of the lighting circuit of a dielectric barrier discharge fluorescent lamp utilizing a push-pull inverter circuit. In addition, Figure 11 is a diagram showing the operation of the inverter circuit presented in Figure 10.

[0004] In Figure 10, reference number 1 denotes a lamp and 2 a boosting transformer. Inverter circuit 3 comprising switch devices Q1, Q2 is connected on the primary winding of boosting transformer 2. Alternating current voltage is applied to the primary side of boosting transformer 2 by alternately turning on switch devices Q1, Q2, and lamp 1 is lit.

[0005] Reference number 11 denotes a sawtooth wave oscillator. The sawtooth wave shown in Figure 11 (a) that is output by sawtooth wave oscillator 11 is input to comparator Cmp. Comparator Cmp compares aforementioned sawtooth wave with the voltage Vs at a fixed level, and generates output when the sawtooth wave exceeds a fixed level signal Vs. For this reason, a pulse signal having a prescribed cycle is output as shown in Figure 11 (b) from comparator Cmp when a sawtooth wave is input. This pulse signal is input to clock terminal CLK of flipflop FF of gate signal generation circuit 4 and flipflop FF is inverted as shown in Figure 11 (c) by this pulse signal.

[0006] The output Q of flipflop FF and its inverted output Q' (a horizontal line is appended over Q in the diagram, the same hereinafter) are input to the input terminals of gate circuits G1, G2, and the pulse signal output by aforementioned comparator Cmp is input to the other input terminal of aforementioned gate circuits G1, G2.

[0007] Accordingly, a 2-phase pulse signal is output from gate circuits G1, G2, as shown in Figure 11 (d) (e), and switch devices Q3, Q4 are alternately turned on by this 2-phase pulse signal. The output of switch devices Q3, Q4 is applied to the gate terminals of aforementioned switch devices Q1, Q2 via resistors R1, R2 as gate signals GU, GL for inverter circuits. By so doing, switch devices Q1, Q2 are alternately turned on, voltage is applied to lamp 1 as shown in Figure 11 (f) and lamp 1 is lit.

[0008] Since light emission of the dielectric barrier discharge fluorescent lamp (hereinafter abbreviated lamp) is pulse light emission rather than continuous light, the following problems arise when it is used as the light source of image readout devices.

[0009] Specifically, if the processing cycle of an image input means such as a CCD is not synchronized with the inverter oscillation of a power supply device that supplies power to a dielectric barrier discharge fluorescent lamp, the light emission pulse number participating in image readout would not be constant per processing cycle of an image input means such as a CCD, and the brightness of the image that is read per processing cycle of an image input means such as a CCD would change. The mode of this change would be periodic based on the beat of the processing cycle of an image input means such as a CCD and of inverter oscillation. Accordingly, the image that is read would contain striplike unevenness.

[0010] When a power supply device using a flyback inverter circuit is used, synchronization of the two is easily completed by initializing oscillation of an inverter oscillator via an external synchronization signal that exhibits a specific phase (for example, initial timing of the readout cycle) in the processing cycle of an image input means such as a CCD.

[0011] However, various problems arise as explained below following initialization of an oscillator by an external synchronization signal and synchronization of the two in full-bridge, half-bridge and push-pull inverter circuits. Please consult the gazette of Japanese Kokai Publication Hei-10-78529 (GP 1001661A1) proposed previously by the inventors concerning the structure of inverter circuits including aforementioned flyback, full-bridge and half-bridge circuits, as well as their operation.

[0012] The lighting circuit shown in aforementioned Figure 10 is explained here.

[0013] (1) The oscillation phase of inverter oscillators and the synchronization signal Sync fluctuate based on various factors. If the two do not overlap, the amount of light would fluctuate based solely on the fluctuation of the light emission cycle, but if the oscillation phases of aforementioned oscillator overlap the external synchronization signal due to fluctuation of the oscillation phase, the amount of light from the lamp would change.

[0014] For example, an external synchronization signal is input, as shown by the broken line in Figure 10, when synchronizing the processing cycle of an image input means such as a CCD with lamp light emission in the lighting circuit shown in Figure 10, and oscillation of a sawtooth wave oscillator must be initialized by an external synchronization signal.

[0015] Here, sawtooth wave oscillator Ocs is initialized by synchronization signal Sync as shown in Figure 12 (a) and oscillation commences after a prescribed period of time when aforementioned external synchronization signal Sync is input at timing (following output of a pulse signal that inverts flipflop FF from comparator Cmp), as shown in aforementioned Figure 12 (a). Accordingly, flipflop FF is inverted as shown in Figure 12 (c). As a result, a gate signal as shown in Figure 12 (d)

(e) is input to the gate terminal of switch devices Q1, Q2 of an inverter circuit and lamp 1 is lit just as in the case shown in aforementioned Figure 11.

[0016] In contrast, sawtooth wave oscillator Ocs is initialized before the sawtooth wave reaches the fixed level of voltage Vs, as shown in Figure 13 (a), when external synchronization signal Sync is input at the timing shown in Figure 13, and pulse signal A that inverts aforementioned flipflop FF is lost. Thus, the output of flipflop FF becomes the output shown in Figure 13 (c). The timing at which switch devices QI, Q2 turn on adopts the shape shown in Figure 13 (d)(e). Consequently, the optical power of the lamp decreases.

[0017] Usually, the frequency of external synchronization signal Sync and the oscillation frequency of aforementioned sawtooth wave oscillator are adjusted since the pulse oscillation phase/frequency fluctuate due to various factors. Even if aforementioned sawtooth wave oscillator is synchronized to a certain extent by external synchronization signal Sync, the oscillation phase of the oscillator will occasionally overlap external synchronization signal Sync.

[0018] The light emission of the lamp would fluctuate if the oscillation phase of the oscillator and external synchronization signal Sync alternate between overlapping and not overlapping due to fluctuation of the oscillation phase of the oscillator and of external synchronization signal

[0019] Sync.

[0020] (2) Furthermore, the ON duration of switch devices Q1 (or Q2) would contract, as shown in Figure 14 (a)-(d), when external synchronization signal Sync and the oscillation phase of the sawtooth wave oscillator overlap, and great surge voltage would be applied to switch devices Q1 (or Q2). The reasons for this are as follows.

[0021] The dielectric barrier discharge fluorescent lamp operates as a capacitor in terms of electrical circuitry, and great current flows only for a period when the voltage applied to the lamp changes or for a period immediately after the change. Accordingly, great current flows immediately after switch devices Q1, Q2 turn ON, but current that increases slowly dependent on the size of the inductance on the primary side of boosting transformer 2, so-called excitation current only, flows thereafter. This current is very small compared to the pulse current that flows immediately after aforementioned switch devices turn ON.

[0022] Specifically, the lamp current would become virtually zero when switch devices Q1, Q2 turn OFF if aforementioned switch devices Q1, Q2 are ON for a duration of time exceeding that required to change the lamp that operates as a capacitor.

[0023] However, when current flows through the lamp, it would be obstructed by switch devices Q1,

[0024] Q2 if the ON duration of switch devices Q1, Q2 is contracted, as shown in Figure 14. For this reason, great surge voltage would be applied to switch devices Q1, Q2.

[0025] When a circuit that controls feedback of the input voltage +V through inverter circuit 3 as well as the current flowing through lamp 1 is mounted (discussed below) to stabilize the optical power of the lamp, the pulse signal that inverts aforementioned flipflop is repeatedly lost and not lost, which brings about instability in the feedback control circuit, thereby creating great optical fluctuation.

[0026] Aforementioned problems arise in half-bridge and full-bridge inverter circuits as well as in push-pull inverter circuits.

[0027] As indicated above, problems such as fluctuation in the optical power and surge in switch devices arise when an oscillator is initialized by an external synchronization signal in push-pull, half-bridge and full-bridge inverter circuits.

[0028] The present invention was completed in light of aforementioned circumstances. It provides a light source device that is ideal for use as the light source of image readout devices in which a dielectric barrier discharge fluorescent lamp can emit light synchronized with an external synchronization signal without attendant fluctuation in the optical power.

Disclosure of Invention

[0029] The present invention solves aforementioned problems as follows.

(1) In a light source device using a dielectric barrier discharge fluorescent lamp that emits light utilizing ultraviolet light generated by dielectric barrier discharge, an inverter oscillator of a power supply device that supplies power to said dielectric barrier discharge fluorescent lamp functions as a variable frequency oscillator. The variable frequency oscillator is controlled so that oscillation signals from said variable frequency oscillator are phase locked with an external synchronization signal.

(2) An internal phase signal in which the periodic amplitude is roughly constant is generated at a specific phase of oscillation of a variable frequency oscillator of an inverter in aforementioned (1), and oscillation of the oscillator is initialized by an external synchronization signal. The voltage of the variable frequency oscillator is controlled as a function of the length of the periods when the effective duration of the external synchronization signal and the effective duration of aforementioned internal phase signal overlap and do not overlap. Oscillation of the variable frequency oscillator is phase locked by controlling the oscillation frequency of the frequency oscillator.

[0030] The oscillator of an inverter of a power supply device that supplies power to a dielectric barrier dis-

charge fluorescent lamp in the present invention functions as a variable frequency oscillator, as mentioned above, and the variable frequency oscillator is controlled so that the oscillation signal from said variable frequency oscillator would be phase locked with an external synchronization signal. Accordingly, the processing cycle of an image input means such as a CCD can be synchronized with oscillation of an inverter circuit and the light emission pulse number that participates in image readout can be held constant per processing cycle of an image input means such as a CCD. In addition, fluctuation of the optical power due to overlapping of the oscillation phases of an inverter oscillator and an external synchronization signal, as shown in aforementioned Figures 13 and 14, can be prevented.

[0031] Furthermore, an internal phase signal in which the periodic amplitude is roughly constant is generated at a specific phase of oscillation of a variable frequency oscillator of an inverter, oscillation of the oscillator is initialized by an external synchronization signal, the voltage of the variable frequency oscillator is controlled as a function of the length of the periods when the effective duration of the external synchronization signal and the effective duration of aforementioned internal phase signal overlap and do not overlap, and the oscillation frequency of the frequency oscillator is controlled, thereby permitting phase locking of the oscillation phase of the inverter to the external synchronization signal without use of a frequency divider. Consequently, the device can be completed inexpensively. Furthermore, the frequency range of the external synchronization signal is not restricted as a function of the variable range of the oscillation frequency of the variable frequency oscillator.

Brief Description of Drawings

[0032] Figure 1 is a diagram showing the overall structure of a light source device in a first working example of the present invention. Figure 2 is a diagram showing the operation of the working example presented in Figure 1. Figure 3 is a diagram showing a second working example of the present invention. Figure 4 is a diagram showing the detailed structure of the second working example of the present invention. Figure 5 is a diagram showing the structure of the phase lock circuit in Figure 4. Figure 6 is a diagram showing the sawtooth wave oscillator of Figure 4 with the phase lock circuit of Figure 4. Figure 7 is a diagram showing each part of the waveform in the matched phase state of the circuit shown in Figure 6. Figure 8 is a diagram showing each part of the waveform in the phase advanced state of the circuit shown in Figure 6. Figure 9 is a diagram showing each part of the waveform in the interrupted state of the circuit shown in Figure 6. Figure 10 is a diagram showing an example of the structure of the lighting circuit of the dielectric barrier discharge fluorescent lamp using a push-pull inverter circuit. Figure 11 is a diagram showing the operation of Figure 10. Figure 12 is a diagram explaining the state in which the external synchronization signal and the inverter oscillation phase do not overlap. Figure 13 is a diagram explaining the state in which the external synchronization signal and the inverter oscillation phase overlap. Figure 14 is a diagram showing the state in which the external synchronization signal and the inverter oscillation phase overlap when the switch device ON duration of the inverter is short.

[0033] Figure 1 is a diagram showing the overall structure of a light source device in a first working example of the present invention. Reference number 5 denotes a DC power source. The direct current voltage output by DC power source 5 is supplied to inverter circuit 3 which switches this direct current voltage and converts it to alternating current. The alternating current voltage output by inverter circuit 3 is boosted by boosting transformer 2 and supplied to dielectric barrier discharge fluorescent lamp 1. The push-pull inverter circuit shown in aforementioned Figure 10 as well as half-bridge or full-bridge inverter circuits can be used as inverter circuit 3.

[0034] Reference number 4 denotes a gate signal generation circuit while reference number 11 denotes a variable frequency oscillator. A circuit provided with the same flipflop as that shown in aforementioned Figure 10 may be used as gate signal generation circuit 4, while MC4024, an IC produced by Motorola Corp. may be used as variable frequency oscillator 11.

[0035] The oscillation signal output from variable frequency oscillator 11 is input to gate signal generation circuit 4 to generate the gate signal that drives the switch device of inverter circuit 3.

[0036] The oscillation signal output by aforementioned variable frequency oscillator 11 is divided by frequency divider 12 and is then input to phase comparator 13. Phase comparator 13 compares the output of frequency divider 12 with the phase of external synchronization signal Sync and then outputs the comparison results to low-pass filter 14 that operates as an error integrator. Low-pass filter 14 integrates the output of phase comparator 13 and generates output in response to aforementioned phase difference. MC4044, an IC produced by Motorola Corp. that houses these together, can be used as aforementioned phase comparator 13 and low-pass filter 14.

[0037] The output of low-pass filter 14 is input to the frequency- controlled input terminal of variable frequency oscillator 11. Variable frequency oscillator 11 oscillates at a frequency in response to the output of low-pass filter 14, with the result that the oscillation signal from variable frequency oscillator 11 is locked to the phase of external synchronization signal Sync. As a result of such a structure, variable frequency oscillator 11 oscillates at a frequency that is multiplied only by the divide ratio of frequency divider 12 to the frequency of external synchronization signal Sync, and synchronized with external synchronization signal Sync.

[0038] Figure 2 is a diagram showing the operation of the working example presented in Figure 1. Figure 2 ex-

plains the operation of the working example shown in Figure 1.

[0039] Variable frequency oscillator 11 outputs the oscillation signal shown in Figure 2 (a). This oscillation signal is divided by frequency divider 12 which then generates output as shown in Figure 2 (b).

[0040] When external synchronization signal Sync is input to phase comparator 13 as shown in Figure 2 (c), phase comparator 13 compares external synchronization signal Sync (for example, its rise) with the oscillation signal (for example, its rise) of variable frequency oscillator 11 and then generates output in response to the phase difference as shown in Figure 2 (d). The output of phase comparator 13 is input to low-pass filter 14 which then integrates the output of phase comparator 13 and generates output as shown in Figure 2 (e).

[0041] The output of low-pass filter 14 is input to the frequency-controlled input terminal of variable frequency oscillator 11. Variable frequency oscillator 11 oscillates at a frequency in response to the voltage that is input to the frequency-controlled input terminal.

[0042] When the oscillation signal of variable frequency oscillator 11 is retarded by external synchronization signal Sync, the output of low-pass filter 14 is raised, as shown in Figure 2 (e), and the oscillation frequency of variable frequency oscillator 11 is raised. Furthermore, when the oscillation signal of variable frequency oscillator 11 is advanced by external synchronization signal Sync, the output of low-pass filter 14 is lowered, as shown in Figure 2 (e), and the oscillation frequency of variable frequency oscillator 11 is lowered. As a result, the phase of the oscillation signal of variable frequency oscillator 11 is phase locked with the external synchronization signal.

[0043] On the other hand, the oscillation signal of variable frequency oscillator 11 is input to gate signal generation circuit 5 which then outputs a gate signal that drives the switch devices of inverter circuit 3 based on aforementioned oscillation signal.

[0044] The switch devices of inverter circuit 3 open/close as a function of the gate signal and converts the direct current voltage that is output by DC power source 5 to alternating current voltage. The alternating current voltage that is output by inverter circuit 3 is applied to lamp 1 via boosting transformer 2 and then lights lamp 1.

[0045] Light emission of lamp 1 can be synchronized with external synchronization signal Sync since the oscillation phase of the oscillation signal that is input to gate signal generation circuit 5 is phase locked to external synchronization signal Sync as mentioned above. Furthermore, the fluctuation of optical power shown in aforementioned Figures 13 and 14 can be prevented since external synchronization signal Sync does not overlap the oscillation phase of the oscillator, as mentioned above.

[0046] The processing cycle of an image input means such as a CCD can be synchronized with oscillation of inverter circuit 3 since variable frequency oscillator 11 is controlled so that oscillation of variable frequency oscillator 11 is phase locked to external synchronization signal Sync in this working example. The light emission pulse number that participates in image readout becomes constant per processing cycle of an image input means such as a CCD. As a result, the brightness of the image that is read per processing cycle of an image input means such as a CCD does not change.

[0047] Incidentally, installation of frequency divider 12 as in aforementioned first working example permits the frequency multiplication ratio to be accurately determined but it also raises the cost. In addition, the frequency range of the external synchronization signal is restricted as a function of the variable range of the oscillation frequency of variable frequency oscillator 11. A further defect is that the divide ratio of frequency divider 12 must be set as a function of the variable frequency range of the external synchronization signal.

[0048] The oscillation signal of a variable frequency oscillator is phase locked to the external synchronization signal without using a frequency divider in a second working example of the present invention shown here.

[0049] An internal phase signal in which the periodic amplitude is roughly constant is generated at a specific phase of oscillation of a variable frequency oscillator of an inverter in the second working example of the present invention, and oscillation of the oscillator is initialized by an external synchronization signal. Out of the effective durations of the external synchronization signal, the duration of overlap with the effective duration of the internal phase signal raises the frequency of the variable frequency oscillator while the duration of no overlap with the effective duration of the internal phase signal out of the effective durations of the external synchronization signal lowers the frequency of the variable frequency oscillator, resulting in phase lock of oscillation of the variable frequency oscillator to the external synchronization signal.

[0050] Figure 3 is a diagram showing a second working example of the present invention. The sections that are identical with those in Figure 1 are given the same notation. Reference number 1 denotes a dielectric barrier discharge fluorescent lamp, reference number 2 denotes a boosting transformer, reference number 3 denotes an inverter circuit, reference number 4 denotes a gate signal generation circuit, and reference number 5 denotes a DC power source.

[0051] Reference number 11 denotes a variable frequency oscillator that is initialized by external synchronization signal Sync. The oscillation signal that is output by variable frequency oscillator 11 is provided to gate signal generation circuit 4 and is input to pulse generator 21 that generates an internal phase signal in which the periodic amplitude is roughly constant at a specific phase of said oscillation signal.

[0052] The output of pulse generator 21 is input to one input terminal of gate circuits G11, G12, while external synchronization signal Sync is input to the other input

terminal of gate circuits G11, G12. Both input terminals of gate circuit G11 generate output at high level, while gate circuit G12 generates output when the output of pulse generator 21 is at a low level and external synchronization signal Sync is at a high level. The outputs of gate circuits G11, G12 are input to current integration circuit 24 via charge pump 22 and discharge pump 23. Current integration circuit 24 generates voltage in response to the phase difference of external synchronization signal Sync and the output of aforementioned pulse generator 21. This voltage is input to the frequency controlled terminal of variable frequency oscillator 11. The circuit comprising aforementioned pulse generator 21, gate circuits G11, G12, charge pump 22, discharge pump 23, and current integration circuit 24 is termed phase lock circuit 20.

[0053] The operation of this working example is explained below.

[0054] The oscillation signal of variable frequency oscillator 11 is input to gate signal generation circuit 4, as mentioned above, and gate signal generation circuit 4 outputs a gate signal that drives the switch devices of inverter circuit 3 based on aforementioned oscillation signal.

[0055] The switch devices of inverter circuit 3 open/close as a function of the gate signal and the direct current voltage that is output by DC power source 5 is converted to alternating current voltage. The alternating current voltage that is output by inverter circuit 3 is applied to lamp 1 via boosting transformer 2, thereby lighting the lamp.

[0056] On the other hand, the oscillation signal of variable frequency oscillator 11 is input to pulse generator 21 which then generates an internal phase signal in which the periodic amplitude is roughly constant at a specific phase of said oscillation signal.

[0057] Gate circuit G11 generates output when aforementioned internal phase signal is at a high level and the external synchronization signal is at a high level. It operates charge pump 22 for current integration circuit 24 and raises the output. In addition, gate circuit G12 generates output when the internal phase signal is at a low level and the external synchronization signal is at a high level. It operates discharge pump 23 for current integration circuit 24 and reduces the output.

[0058] Consequently, the output voltage of current integration circuit 24 is unchanged when the period during which the internal phase signal is at a high level and the external synchronization signal is at a high level is equal to the period during which the internal phase signal is at a low level and the external synchronization signal is at a high level.

[0059] On the other hand, when the internal phase signal reaches a phase that is more advanced than the external synchronization signal, the durations of low level internal phase signal and high level external synchronization signal become longer, and the output voltage of current integration circuit 24 falls. Accordingly, the oscillation frequency of variable frequency oscillator 11 falls.

[0060] Accordingly, the duration of high level internal phase signal and high level external synchronization signal becomes equal to the duration of low level internal phase signal and high level external synchronization signal.

[0061] Conversely, when the internal phase signal reaches a phase that is more retarded than the external synchronization signal, the durations of low level internal phase signal and high level external synchronization signal become shorter and the output voltage of current integration circuit 24 rises. For this reason, the oscillation frequency of variable frequency oscillator 11 rises and the duration of high level internal phase signal and high level external synchronization signal becomes equal to the duration of low level internal phase signal and high level external synchronization signal. As indicated above, the oscillation frequency of variable frequency oscillator 11 is controlled as a function of the phase difference between external synchronization signal Sync and the internal phase signal, and the oscillation signal of variable frequency oscillator 6 becomes phase locked with the external synchronization signal.

[0062] Fluctuation of the optical power can be prevented with no overlapping of external synchronization signal Sync with the oscillation phase of the oscillator, just as in aforementioned first working example, since variable frequency oscillator 11 is controlled so as to phase lock variable frequency oscillator 11 to external synchronization signal Sync in this working example, as indicated above. Furthermore, the processing cycle of an image input means such as a CCD is synchronized with the inverter of a power supply device so that the light emission pulse number that participates in image readout becomes constant per processing cycle of an image input means such as a CCD. Accordingly, the brightness of images that are read per processing cycle of an image input means such as a CCD does not change.

[0063] Furthermore, a more inexpensive structure can be completed since the oscillation signal of variable frequency oscillator 11 can be phase locked to the external synchronization signal without using a frequency divider. In addition, the frequency range of the external synchronization signal is not restricted as a function of the variable range of the oscillation frequency of variable frequency oscillator 11.

[0064] Next, a concrete constituent example of aforementioned second working example is explained using Figures 4 and 5.

[0065] Figure 4 is a diagram showing the overall structure of a light source device in this working example. Figure 5 shows the circuit structure of phase lock circuit 20 in Figure 4.

[0066] The basic structures of inverter circuit 3 and gate signal generation circuit 4 in this working example are identical with those shown in aforementioned Figure

10. A push-pull inverter circuit was explained in Figure 4, but a full-bridge or half-bridge circuit as mentioned above may be used as inverter circuit 3.

[0067] First, each part of the circuit shown in Figure 4 is explained here.

(1) Chopper circuit, gate generation circuit and inverter circuit

[0068] DC voltage Vi supplied from the DC voltage source that is not illustrated is connected to switch device Q5 utilizing FET, etc., via capacitor C1 and choke coil CH in Figure 4.

[0069] When switch device Q5 changes from ON to OFF, the induction voltage generates at choke coil CH is accumulated in smoothing capacitor C2 via diode D1 as boosted DC voltage Vj. The chopper circuit comprising aforementioned choke coil CH, switch device Q5, diode D1 and smoothing capacitor C2 is generally termed a boosting chopper circuit. A snubber circuit for surge absorption comprising capacitor C3 and resistor R3, etc., is optionally mounted in switch device Q5 for a chopper circuit.

[0070] The push-pull inverter circuit shown in aforementioned Figure 10 comprises switch devices Q1, Q2 utilizing FET, etc., as well as boosting transformer 2. The output voltage Vj of aforementioned chopper circuit is connected to the central tab on the primary side of boosting transformer 2.

[0071] Voltage is applied to lamp 1 as shown in aforementioned Figure 11 (f) and lamp 1 is lit when switch devices Q1, Q2 alternately turn ON.

[0072] The output of sawtooth wave oscillator 11 that generates sawtooth waves having frequency in response to the voltage applied to the frequency controlled terminal is input to one input terminal of comparator Cmp. Output voltage Vs from operational amplifier Amp is input to the other input terminal of comparator Cmp. A square-wave oscillation signal in which the duty cycle ratio shown in aforementioned Figure 11 (b) is modulated as a function of the high-low relation between the output sawtooth wave of variable frequency oscillator 11 and the output voltage Vs from aforementioned operational amplifier Amp is output from comparator Cmp.

[0073] The oscillation signal output from comparator Cmp is input to gate signal generation circuit 4 comprising flipflop FF, gate circuits G1, G2, switch devices Q3, Q4. Gate signals GU, GL for the inverter circuit are generated as a result. Gate signals GU, GL for the inverter circuit are input to the gate terminals of switch devices Q1, Q2 via respective resistors R1, R2.

[0074] On the other hand, the chopper gate signal generation circuit is constructed using a signal adder comprising diodes D2, D3 and resistors R4. Gate signal Gc for the chopper circuit is generated by input of gate signals GU, GL for the inverter circuit thereto. The method of generating signals synchronized with gate signals GU, GL for the inverter circuit is one of the simplest methods of generating gate signal Gc for a chopper circuit via aforementioned signal adder.

[0075] Gate signal Gc for a chopper circuit is input to the gate terminal of switch device Q5 for aforementioned chopper circuit via buffer circuit comprising total transistors Q6, Q7, differentiation circuit comprising capacitor C4 and resistor R5, and resistor R6.

[0076] Aforementioned buffer circuit comprising total transistors Q6, Q7, differentiation circuit comprising capacitor C4 and resistor R5 are added to reduce the possibility of loss which readily arises when switch device Q5 for the chopper circuit turns ON. They may be optionally omitted.

[0077] The operation of aforementioned switch devices Q1, Q2 for an inverter circuit, comparator Cmp and gate signal generation circuit 4 is identical with that shown in aforementioned Figure 11. The operation of an inverter in this working example and the operation of aforementioned chopper circuit are explained below. Please consult aforementioned Japanese Kokai Publication Hei-10-78529 for details of the operation of aforementioned inverter and of aforementioned chopper circuit.

[0078] Gate signal Gc for a chopper circuit reaches high level when either gate signal GU, GL for the inverter circuit in Figure 4 reaches the high level. Consequently, the frequency of gate signal Gc for the chopper circuit reaches the frequency for circuit operation, specifically, double the frequency of aforementioned switch devices Q1, Q2 for the inverter circuit.

[0079] Switch device Q5 for aforementioned chopper circuit turns ON when gate circuit Gc for the chopper circuit reaches a high level. The current through aforementioned choke coil CH increases and magnetic energy accumulates in choke coil CH. When gate signal Gc of aforementioned chopper circuit reaches the low level, switch device Q5 for aforementioned chopper circuit turns OFF and current through aforementioned choke coil CH decreases. Magnetic energy accumulated in choke coil CH charges aforementioned smoothing capacitor C2 as electrical energy.

[0080] On the other hand, when one of two gate signals GU, GL for the inverter circuit reaches the high level, one of the corresponding switch devices Q1, Q2 turns ON and the voltage waveform imposed on the lamp steeply changes in the direction of polarity reversal at the secondary side of boosting transformer 2. Discharge is then generated at lamp 1.

[0081] As mentioned above, current flows in pulses to switch devices Q1 or Q2 and to lamp 1 immediately after one of the two switch devices Q1, Q2 turns ON since lamp 1 functions overall as a capacitor, but after the end of discharge, there is no significant current flow to the lamp.

[0082] Accordingly, even if one of two switch devices Q1, Q2 for the inverter circuit turns ON after discharge ends, only current that increases slowly dependent on the size of inductance on the primary side of boosting

transformer 2, so-called excitation current, would flow to switch devices Q1, Q2. This is quite small compared to the pulse current that flows immediately after the switch devices for aforementioned inverter circuit turns ON.

[0083] In short, the voltage output from aforementioned chopper circuit is virtually constant since the charge flowing out from aforementioned smoothing capacitor C2 is slight after the end of pulse current that flows immediately after switch devices Q1, Q2 turn ON.

(2) Feedback stabilization circuit of lamp feed power

[0084] A feedback stabilization control function of the lamp feed power that is included in the circuit shown in Figure 4 is explained here.

[0085] The power source for gate signal generation circuits, etc., or controlling circuits for feedback stabilization control, etc., decreases as a result of the steep power-source peak current that accompanies operation of the chopper circuit due to diode D5 and capacitor C5, and it is supplied to reference voltage source VReg. Capacitor C6 is connected on the output side of reference voltage source VReg which then generates reference voltage VRef for feedback stabilization control.

[0086] On the other hand, chopper circuit output voltage Vj is detected as the object of feedback stabilization control by diode D6, capacitor C7, variable resistor VR1, resistor R7. Diode D6, capacitor C7 comprise the pick-hold circuit which removes ripples in chopper circuit output voltage Vj.

[0087] The detected chopper circuit output voltage is input to the non-inverted input terminal of aforementioned operational amplifier Amp. On the other hand, the output voltage of reference voltage source VS is divided by resistors R8, R9, and is input to the inverted input terminal of aforementioned operational amplifier Amp. Feedback capacitor C8 is connected between the output terminal and the inverted input terminal to operate as an error integration circuit in operational amplifier Amp.

[0088] In this working example, a circuit structure is provided to control feedback stabilization of aforementioned structure. The output voltage of operational amplifier Amp is raised when the input voltage to the non-inverted input terminal of aforementioned operational amplifier Amp is higher than the input voltage to the inverted input terminal.

[0089] For this reason, the duty ratio of the oscillation signal from aforementioned comparator Cmp falls. Specifically, the duration of two low level gate signals increases while the duty ratio of the duration when switch device Q5 for the chopper circuit is ON declines. As a result, chopper circuit output voltage Vj declines.

[0090] Conversely, chopper circuit output voltage Vj is raised when the input voltage to the noninverted input terminal of aforementioned operational amplifier Amp is lower than the input voltage to the inverted input terminal.

[0091] Specifically, chopper circuit output voltage Vj is controlled at a constant, with the result that the lamp input voltage is subjected to constant feedback stabilization control. Furthermore, the lamp input voltage can be altered by adjusting aforementioned variable resistor VR1.

[0092] The oscillation signal duty ratio fluctuates accompanying aforementioned feedback operation, with the result that the duty ratio of switch devices Q1, Q2 for the inverter circuit fluctuates. However, current flows in pulses immediately after one of switch devices Q1, Q2 turns ON since lamp 1 basically operates as a capacitor, as mentioned above, but after discharge is completed, there is no significant flow of current to the lamp. For this reason, fluctuation in aforementioned duty cycle poses no problems with discharge of the lamp itself or with power applied to the lamp.

[0093] However, problems associated with this can be resolved utilizing the invention presented in Japanese Kokai Publication Hei-11-105884 that was previously proposed by the inventors.

[0094] Among the circuit devices used to construct the light source device in the working example shown in Figure 4, integrated circuit IC7 (stated in Figure 6) that houses aforementioned sawtooth wave oscillation circuit 11, voltage comparator Cmp, operational amplifier Amp, flipflop FF, gate circuits G11, G12, transistors Q3, Q4, reference voltage source Vs, etc., in a single package has been marketed (for example, TL 494 from Texas Instruments). Aforementioned circuit can be manufactured with far fewer components by using this.

(3) Phase locked circuit

[0095] The oscillation frequency of aforementioned sawtooth wave oscillator 11 is controlled by the voltage that is input to the frequency control terminal, and the oscillation phase is controlled so as to be synchronized with external synchronization signal Sync. Accordingly, phase lock circuit 20 is mounted in this working example as shown in Figure 4.

[0096] Transistor Q8 is connected to the frequency controlled terminal of sawtooth wave oscillator 11 shown in Figure 4. Frequency controlled signal FC that is output by phase lock circuit 20 is input to aforementioned transistor Q8. The oscillation frequency of sawtooth wave oscillator 11 is controlled as a function of the magnitude of aforementioned frequency controlled signal FC. In addition, external capacitor 9 is attached in sawtooth wave oscillator 11 to establish the oscillation frequency. The oscillation of sawtooth wave oscillator 11 is initialized by discharge of capacitor C9.

[0097] Figure 5 is a diagram showing the structure of aforementioned phase lock circuit 20.

[0098] Initialization signal Sync is input to the synchronization signal input terminal Sync in Figure 5, and is input to switch device Q9 shown in Figure 4. In addi-

tion, the oscillation signal of sawtooth wave oscillator 11 is input to the input terminal Osc of phase lock circuit 20 shown in Figure 5.

[0099] Phase lock circuit 20 shown in Figure 5 has the same function as that of the phase lock circuit shown in aforementioned Figure 3. It is provided with a circuit corresponding to pulse generator 21 having a phase lock circuit in Figure 3 (circuit comprising IC1, capacitor C11, IC2, etc., shown in Figure 5), a circuit corresponding to gate circuits G11, G12 (logic circuit comprising diodes D13, D14 shown in Figure 5), a circuit corresponding to charge pump 22, discharge pump 23 (circuit comprising diodes D15, D16 shown in Figure 5), and a circuit corresponding to current integration circuit 24 (circuit comprising capacitor C12, etc.). The oscillation phase of sawtooth wave oscillator 11 locked by initialization signal Sync through the same operations as those explained in aforementioned Figure 3. Furthermore, phase lock circuit 20 shown in Figure 5 is provided with start/stop circuit 30 that discontinues operation once start signal ACT reaches a low level.

[0100] Figure 6 shows a circuit comprising phase lock circuit 20 shown in aforementioned Figures 4, 5 and sawtooth wave oscillator 11 that is integrated in one board. The sections that are identical with those in Figures 4, 5 are given the same notation. The phase lock circuit is explained below using Figure 6. The sawtooth wave oscillator in Figure 6 is a block denoted by reference number 11 in IC7.

[0101] Reference number 30 in Figure 6 denotes a start/stop circuit. When the start signal ACT* is at a high level (shutdown state), the output ACT of start/stop circuit 30 is at a low level and the output of logic inversion circuit IC6 is at a high level. As a result, the output side of resistors R13, R15 is clamped at a high level via diodes D11, D12, and the circuit control operation is shut down. On the other hand, when the start signal ACT* is at a low level, the output ACT of start/stop circuit 30 is at a high level and the output of logic inversion circuit IC6 is at a low level. As a result, circuit operations can continue. Below, circuit operation is explained with aforementioned start signal ACT* at a low level and continuation of circuit operations permitted.

[0102] The oscillation signal from sawtooth wave oscillator 11 is input to logic inversion circuit IC1. Logic inversion circuit IC1 generates low level output that exceeds the fixed level of amplitude of the sawtooth wave oscillation signal. The pulse signal output by logic inversion circuit IC1 is differentiated by a differentiation circuit comprising capacitor C11 and resistor R12 and is input to logic inversion circuit IC2 via resistor R11. Logic inversion circuit IC2 generates low level output when the differentiation waveform output by aforementioned differentiation circuit exceeds a fixed level. Specifically, logic inversion circuit IC2 outputs a pulse signal in which the pulse amplitude is roughly fixed and in which the frequency is equal to the oscillation frequency of aforementioned sawtooth wave oscillator 11.

[0103] This pulse signal is then inverted by logic inversion circuit IC3. The circuit comprising aforementioned logic inversion circuit IC1, differentiation circuit, ..., logic inversion circuit IC3 corresponds to pulse generator 21 shown in aforementioned Figure 3. Below the pulse signal output by logic inversion circuit IC3 is termed the internal phase signal.

[0104] Resistor R14 and diode D13 are connected to the output side of logic inversion circuit IC3 while resistor R15 is connected to the cathode side of diode D13. Furthermore, diode D14 is connected to the output side of resistor R14 while the cathode side of diode D14 is connected to the output side of logic inversion circuit IC5 discussed below.

[0105] External synchronization signal Sync is input to the input of logic inversion circuit IC4. External synchronization signal Sync is a positive logic pulse of 0.5 to 4 μs amplitude.

[0106] The output of logic inversion circuit IC4 is high level when external synchronization signal Sync is not input (at low level) and the output of logic inversion circuit IC5 connected to the output side of logic inversion circuit IC4 is low level. Furthermore, the output of logic inversion circuit IC4 is low level when external synchronization signal Sync is input (at high level), and the output of logic inversion circuit IC5 is high level.

[0107] The output of logic inversion circuit IC4 is connected to the cathode side of diode D13 via resistor R15. Furthermore, the output of logic inversion circuit IC5 is connected to the controlled input terminal of transistor Q8. Transistor Q8 turns ON when external synchronization signal Sync is high level, and capacitor C9 discharges. Sawtooth wave oscillator 11 is initialized as a result.

[0108] The output of logic inversion circuit IC4 is high level when external synchronization signal Sync is not input (at low level), the output of logic inversion circuit IC5 is low level and the output side of aforementioned logic inversion circuit IC3 is clamped at low level. As a result, the internal phase signal that is output by logic inversion circuit IC3 is not input to diode D15.

[0109] Conversely, the output of logic inversion circuit IC4 is low level when external synchronization signal Sync is input (at high level), and the output of logic inversion circuit

[0110] IC5 is high level. Here, current flows to diode D15 via resistor R14 from logic inversion circuit IC3 when the internal phase signal (output of logic inversion circuit IC3) is high level. Furthermore, the potential on the cathode side of diode D16 reaches high level via diode D13 because the output of logic inversion circuit IC3 is high level. As a result, capacitor C12 that is connected at the contact points of diodes D15, D16 is charged. The output side of logic inversion circuit IC3 does not reach low level since resistor R15 is connected to the output side of logic inversion circuit IC4 even though the output side of logic inversion circuit IC4 at this time is low level.

[0111] Furthermore, internal phase signal reaches

low level (output of logic inversion circuit IC3 is low level) when external synchronization signal Sync is high level (output of logic inversion circuit IC4 is low level), and the potential on the anode side of diode D15 becomes low level. Current then flows to logic inversion circuit IC4 via diode D16, resistor R15. As a result, capacitor C12 that is connected at the contact points of diodes D15, D16 is discharged.

[0112] Specifically, the circuit comprising aforementioned logic inversion circuits IC3, IC4, IC5, diodes D13, D14, D15, D16, etc., functions as gates G11, G12, charge pump 22, discharge pump 23 as shown in aforementioned Figure 3, and capacitor C12 functions as current integration circuit 24 shown in Figure 3.

[0113] The voltage of capacitor C12 is input to transistor Q9 and the oscillation frequency of sawtooth wave oscillator 11 is controlled by the output voltage of transistor Q9. In addition, variable resistor VR2 is connected in parallel to transistor Q9, and the oscillation frequency of sawtooth wave oscillator 11 can be adjusted by variable resistor VR2.

[0114] Figures 7, 8, and 9 are waveform diagrams showing the operation in Figure 6. The phase lock operation in this working example is explained using Figures 6 through 9.

(1) Operation in matched phase state

[0115] Figure 7 is a waveform diagram showing the operation when the oscillation phase of sawtooth wave oscillator 11 and external synchronization signal Sync are in the matched phase state. (1) to (13) in the diagram show the waveforms at (1) to (13) in Figure 6.

[0116] Sawtooth wave oscillator 11 outputs sawtooth waves shown in Figure 7 (1). This oscillation signal is input to logic inversion circuit IC1 which generates high level output when the amplitude of the oscillation signal is at a lower than prescribed level. Accordingly, a pulse signal shown in Figure 7 (2) is output from logic inversion circuit IC1.

[0117] The differentiation circuit comprising capacitor C11, resistor R12 differentiates the pulse signal shown in Figure 7 (2). The output waveform is shown in Figure 7 (3). Logic inversion circuit IC2 outputs a pulse signal shown in Figure 7 (4) since logic inversion circuit IC2 generates low level output when the amplitude of the differentiated waveform shown in Figure 7 (3) exceeds a prescribed level.

[0118] The output of logic inversion circuit IC2 is input to logic inversion circuit IC3 via resistor R13 if the output of logic inversion circuit IC6 is low level, as shown in Figure 7 (13), when start/stop signal ACT* is low level (starting state), and the waveforms on the input side and output side of logic inversion circuit IC3 adopt the forms shown in Figure 7 (5)(6). The waveform of Figure 7 (6) is termed an internal phase signal, as mentioned above.

[0119] The pulse signal shown in Figure 7 (2) is differentiated, as mentioned above. The differentiated waveform is compared to a prescribed value in logic inversion circuit IC2, and a pulse signal shown in Figure 7 (4) is generated, thereby permitting the generation of a pulse signal of roughly fixed amplitude that is not dependent on the oscillation frequency of sawtooth wave oscillator 11. A mono-stable multivibrator may be used instead of the differentiation circuit and logic inversion circuit discussed above to generate a fixed-amplitude pulse.

[0120] Transistor Q8 in Figure 6 turns ON, as mentioned above, when external synchronization signal Sync is input at τ time after the sawtooth wave falls as shown in Figure 7, capacitor C9 discharges and sawtooth wave oscillator 11 is initialized. Furthermore, the output of logic inversion circuit IC4 becomes low level, as shown in Figure 7 (7), and the output of logic inversion circuit IC5 becomes high level, as shown in Figure 7 (8).

[0121] At this time, the potential on the anode side of diode D15 which comprises the discharge pump as mentioned above rises, as shown in Figure 7 (9), since the internal phase signal shown in Figure 7 (6) (output of logic inversion circuit IC3) is high level. As a result, current shown in Figure 7 (11) flows to capacitor C12 which comprises the current integration circuit via diode D15. The potential of capacitor C12 rises as shown in Figure 7 (12).

[0122] Next, once the internal phase signal shown in Figure 7 (6) is low level (low level output of logic inversion circuit IC3) when the external synchronization signal is high level, the potential on the anode side of diode D15 falls, as shown in Figure 7 (9). On the other hand, since the potential on the cathode side of diode D16 is low level when the output side of logic inversion circuit IC4 is low level, as shown in Figure 7 (7), current flows out from capacitor C12 which comprises the current integration circuit via diode D16 and the potential of capacitor C12 falls, as shown in Figure 7 (12).

[0123] If the duration during which external synchronization signal Sync is high level and internal phase signal [Figure 7 (6)] is high level is equal to the duration during which external synchronization signal Sync is high level and internal phase signal is low level, the integral values of the charge current and discharge current of capacitor C12 would be equal, and after the potential of capacitor C12 rises, as shown in Figure 7 (12), they would decline by the same amount. As a result, the voltage that is input to the frequency controlled terminal of sawtooth wave oscillator 11 would not change, and the oscillation frequency of sawtooth wave oscillator 11 would not change.

[0124] Specifically, when the oscillation phase of sawtooth wave oscillator 11 and external synchronization signal Sync are in a matched phase state, the device would operate so that the oscillation phase of sawtooth wave oscillator 11 and external synchronization signal Sync are in a prescribed phase relationship, and this state would steadily continue.

(2) Operation in phase advanced state

[0125] Figure 8 is a diagram of the operating waveform when the oscillation phase of sawtooth wave oscillator 11 is in the phase advanced state relative to external synchronization signal Sync. (1) to (13) in the diagram show the waveforms at (1) to (13) in Figure 6.

[0126] If the oscillation phase of sawtooth wave oscillator 11 is in a phase advanced state relative to external synchronization signal Sync for any reason, the duration during which external synchronization signal Sync is high level and the internal phase signal [Figure 8 (6)] is high level would be longer than the duration during which external synchronization signal Sync is high level and the internal phase signal is low level, as shown in Figure 8.

[0127] Since capacitor C12 which comprises the current integration circuit charges when external synchronization signal Sync is high level and the internal phase signal [Figure 8 (6)] is high level, as mentioned above, and discharges when external synchronization signal Sync is high level and the internal phase signal is low level, the charge/discharge current of capacitor C12 in this case would be as shown in Figure 8 (11), and the potential of capacitor C12 would fall, as shown in Figure 8 (12). For this reason, the oscillation frequency of sawtooth wave oscillator 11 would fall and the amount of advance of the oscillation phase of sawtooth wave oscillator 11 relative to external synchronization signal Sync would decrease.

[0128] Thus, the oscillation phase of sawtooth wave oscillator 11 and external synchronization signal Sync would revert to the matched phase state, as shown in Figure 7.

[0129] Conversely, if the oscillation phase of sawtooth wave oscillator 11 should become retarded compared to external synchronization signal Sync, the oscillation frequency of sawtooth wave oscillator 11 would rise and the amount of retardation of the oscillation phase of sawtooth wave oscillator 11 relative to external synchronization signal Sync would decrease.

[0130] For this reason, the oscillation phase of sawtooth wave oscillator 11 and external synchronization signal Sync would revert to the matched phase state, as shown in Figure 7.

(3) Interrupted state

[0131] Figure 9 is a diagram showing the operating state of each section when start/stop signal ACT* is high level and in the interrupted state. (1) to (13) in the diagram show the waveforms at (1) to (13) in Figure 6.

[0132] The output of logic inversion circuit IC6 becomes high level, as shown in Figure 9 (13), when start/stop signal ACT is high level. For this reason, the input side of logic inversion circuit IC3 via diode D11 becomes high level, as shown in Figure 9 (5), and the output side of logic inversion circuit IC3 becomes low level, as shown in Figure 9 (6). Furthermore, the potential on the cathode side of diode D16 via diode D12 becomes high level, as shown in Figure 9 (10). Accordingly, charge (discharge) current would not flow to capacitor C12 even if synchronization signal Sync is input.

[0133] In this state, fixed voltage is applied based on the differential voltage ratio of resistors R16, R17 to the frequency controlled terminal of sawtooth wave oscillator 11, and sawtooth wave oscillator 11 oscillates at a fixed frequency at this voltage.

[0134] If external synchronization signal Sync is input when start/stop signal ACT* is low level, controlled operations take place as explained in Figure 7 and Figure 8, and this is controlled so that the oscillation phase of sawtooth wave oscillator 11 is phase locked to external synchronization signal Sync.

[0135] The present invention can be applied to so-called dielectric barrier discharge excimer lamps that generate ultraviolet light through excimer light emission using rare gases such as neon, argon, krypton, xenon, radon as well as mixtures and compounds of halogens such as arsenic, chlorine or bromine as the discharge gas sealed in lamp 1. In addition, metal vapors such as mercury or mixtures/compounds of these metal vapors with halogens termed metal halides may be effectively used. Any discharge gas that is used can be employed.

[0136] Needless to say, the detailed aspects of circuit operation explained in this working example, for example, signal polarity, or inventive measures such as the selection of specific circuit devices, their addition, omission or modification for reasons of convenience of acquisition or economy, may be energetically pursued in the design of actual devices.

[0137] In particular, measures such as inserting a monostable multiplexer if the pulse amplitude of synchronization signal Sync that is externally input should become problematic or if there is a possibility of the pulse amplitude fluctuating, shaping this to a form having a constant suitable pulse amplitude, or inserting a logic inversion circuit to correct disadvantageous polarity would fall within the scope of the present invention

[0138] The inverter oscillator of a power supply device that supplies power to said dielectric barrier discharge fluorescent lamp in the present invention functions as a variable frequency oscillator, as explained above. It controls the variable frequency oscillator so that the oscillation signal from said variable frequency oscillator is phase locked with an external synchronization signal, thereby permitting lamp light emission to be synchronized with the external synchronization signal. In addition, fluctuation of the optical power due to overlapping of the external synchronization signal and oscillation phase of the oscillator can be prevented.

[0139] For this reason, the light emission pulse number that participates in image readout becomes constant per processing cycle of an image input means such as a CCD. As a result, the brightness of the image that is read per processing cycle of an image input

means such as a CCD does not change.

[0140] An internal phase signal in which the periodic amplitude is roughly constant is generated at a specific phase of oscillation of a variable frequency oscillator of an inverter, and the oscillation frequency of the frequency oscillator is controlled as a function of the length of the duration during which the effective duration of the external synchronization signal and the effective duration of the internal phase signal overlap and do not overlap. Accordingly, the oscillation phase of an inverter can be phase locked to the external synchronization signal without using a frequency divider. This permits the device to be produced inexpensively. Furthermore, the frequency range of the external synchronization signal is not restricted as a function of the variable range of the oscillation frequency of the variable frequency oscillator.

Possibility of industrial utilization

[0141] As mentioned above, the present invention concerns a light source device using a dielectric barrier discharge fluorescent lamp that emits light utilizing ultraviolet light that is generated by dielectric barrier discharge.

Claims

1. A light source device using a dielectric barrier discharge fluorescent lamp that emits light utilizing ultraviolet light that is generated by dielectric barrier discharge in which an inverter oscillator of a power supply device that supplies power to a dielectric barrier discharge fluorescent lamp functions as a variable frequency oscillator, and said variable frequency oscillator is controlled so that the oscillation signal from the variable frequency oscillator is phase locked to an external synchronization signal.

2. The light source device of Claim 1 in which an internal phase signal whose periodic amplitude is roughly constant is generated at a specific phase of oscillation of a variable frequency oscillator of an inverter, oscillation of the oscillator is initialized by an external synchronization signal, and the voltage of the variable frequency oscillator is controlled as a function of the length of the duration during which the effective duration of the external synchronization signal and the effective duration of the internal phase signal overlap and do not overlap, oscillation of the variable frequency oscillator is thus phase locked as a result of control of the oscillation frequency of the frequency oscillator.

FIG. 1

Diagram showing the overall structure of a light source device in a first working example of the present invention.

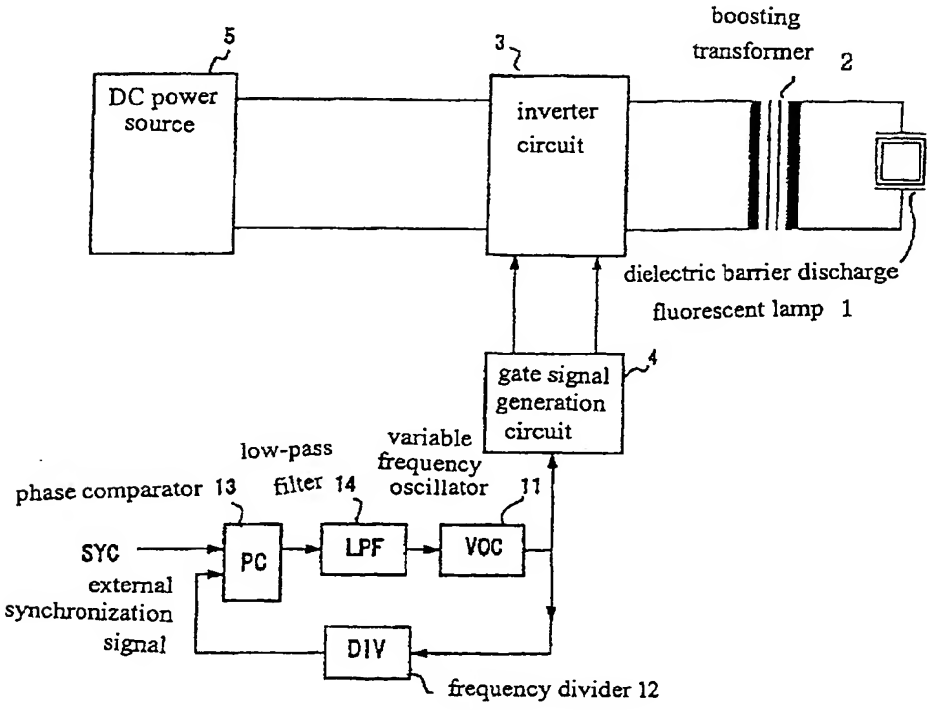


Diagram showing the operation of the working example presented in Figure 1.

FIG. 2(a) VOC output

FIG. 2(b) frequency divider output

FIG. 2(c) external synchronization signal

FIG. 2(d) phase comparator output

FIG. 2(e) low pass filter (error integrator) output

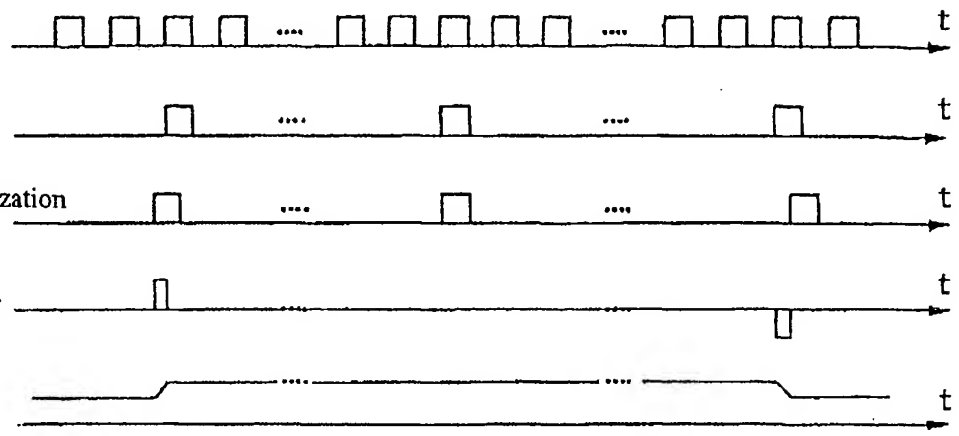


FIG. 3

Diagram showing a second working example of the present invention.

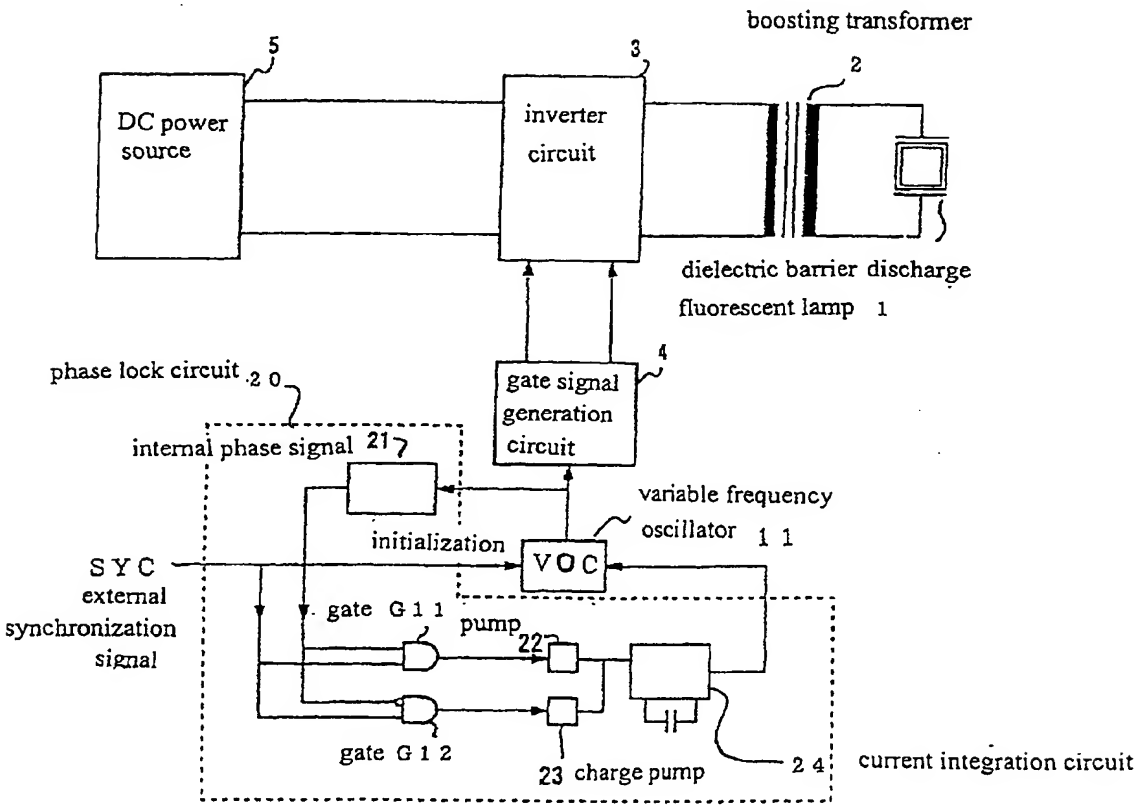


FIG. 4

Diagram showing the detailed structure of the second working example of the present invention.

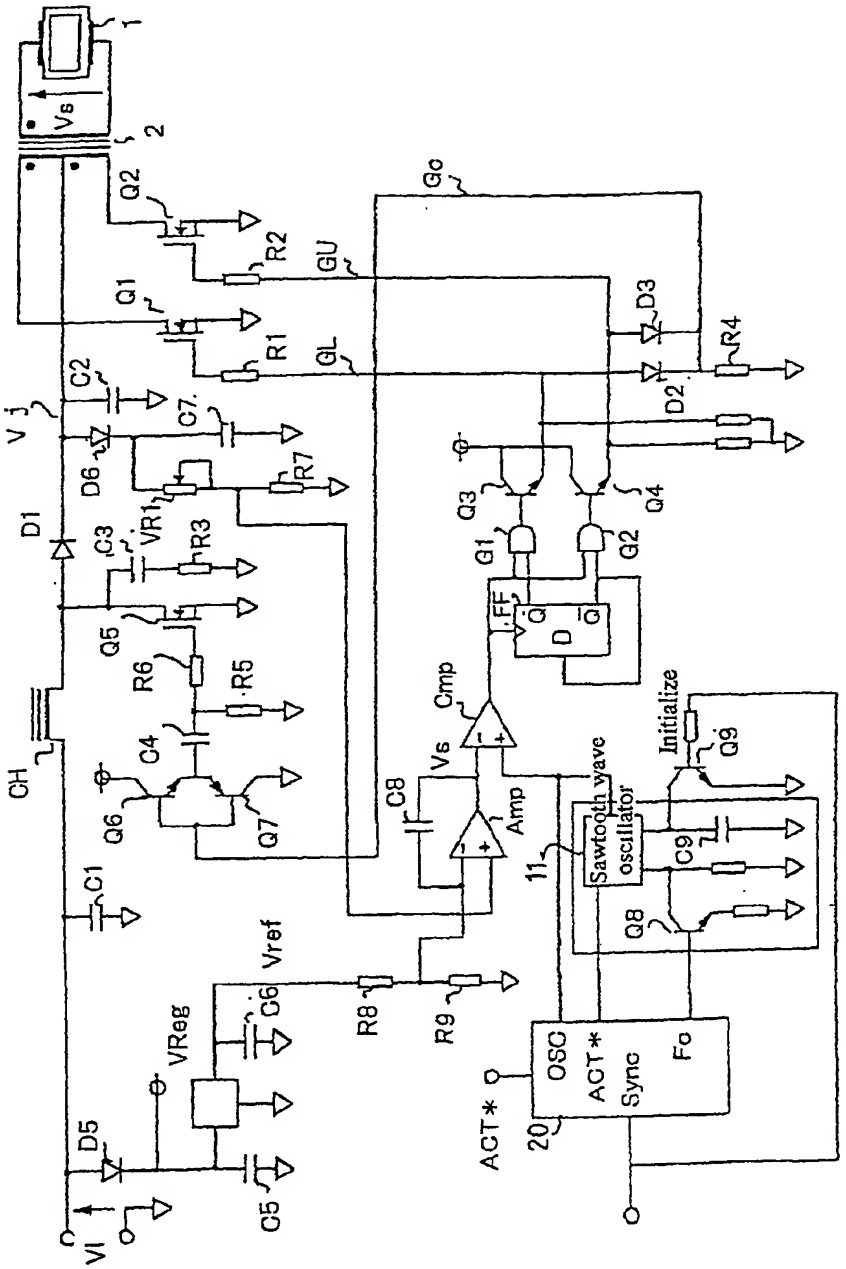


FIG. 5

Diagram showing the structure of the phase lock circuit in Figure 4.

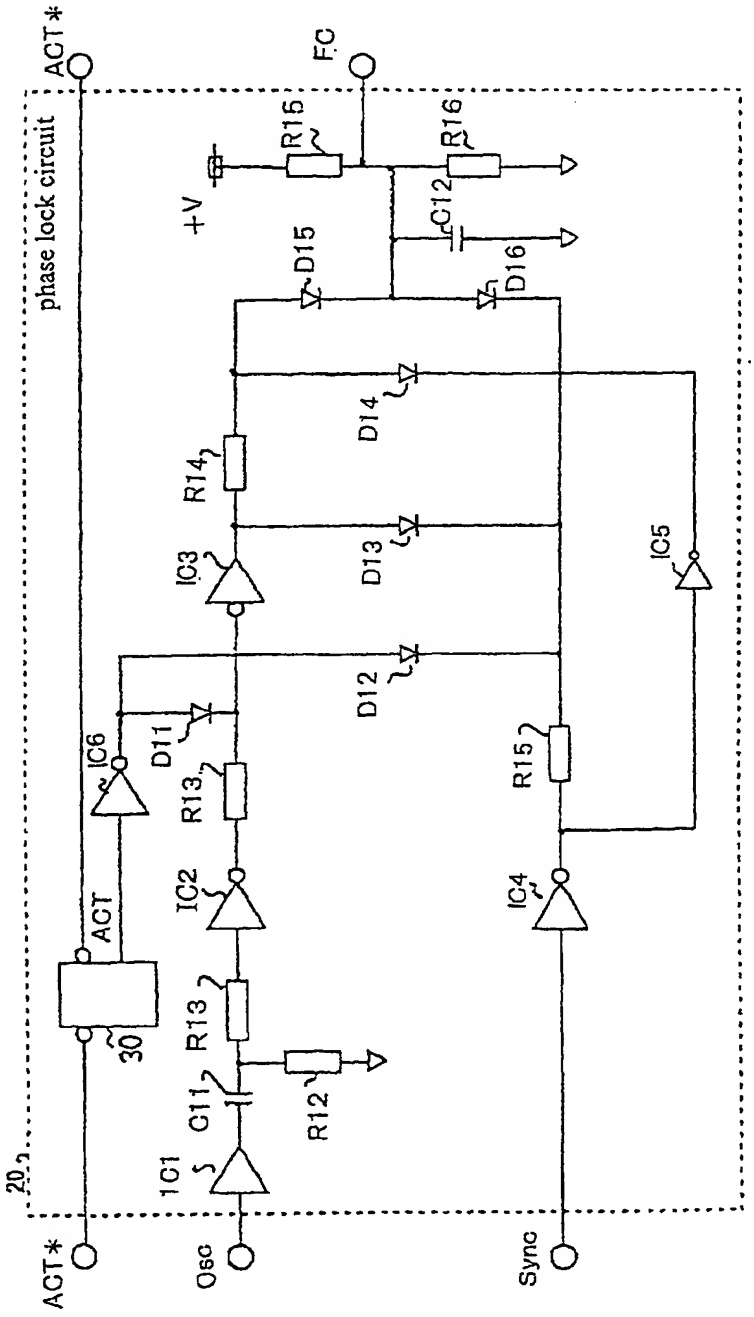


FIG. 6

Diagram showing the sawtooth wave oscillator of Figure 4 with the phase lock circuit of Figure 4.

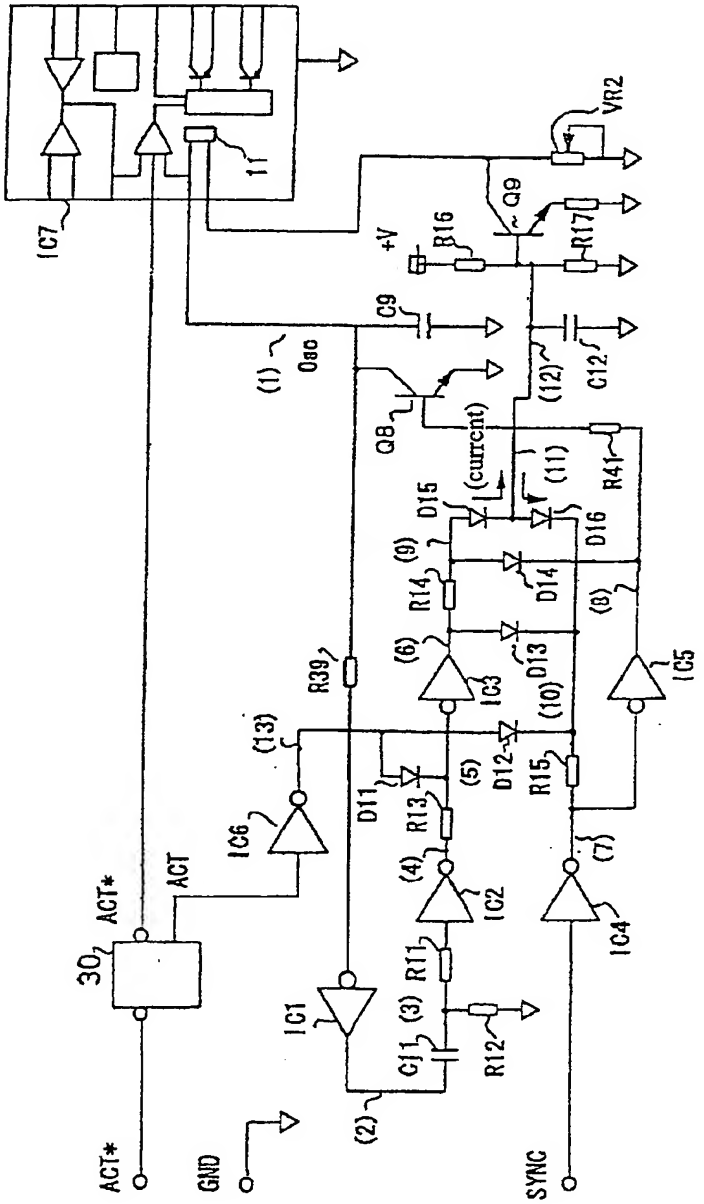


FIG. 7

Diagram showing each part of the waveform in the matched phase state of the circuit shown in Figure 6.

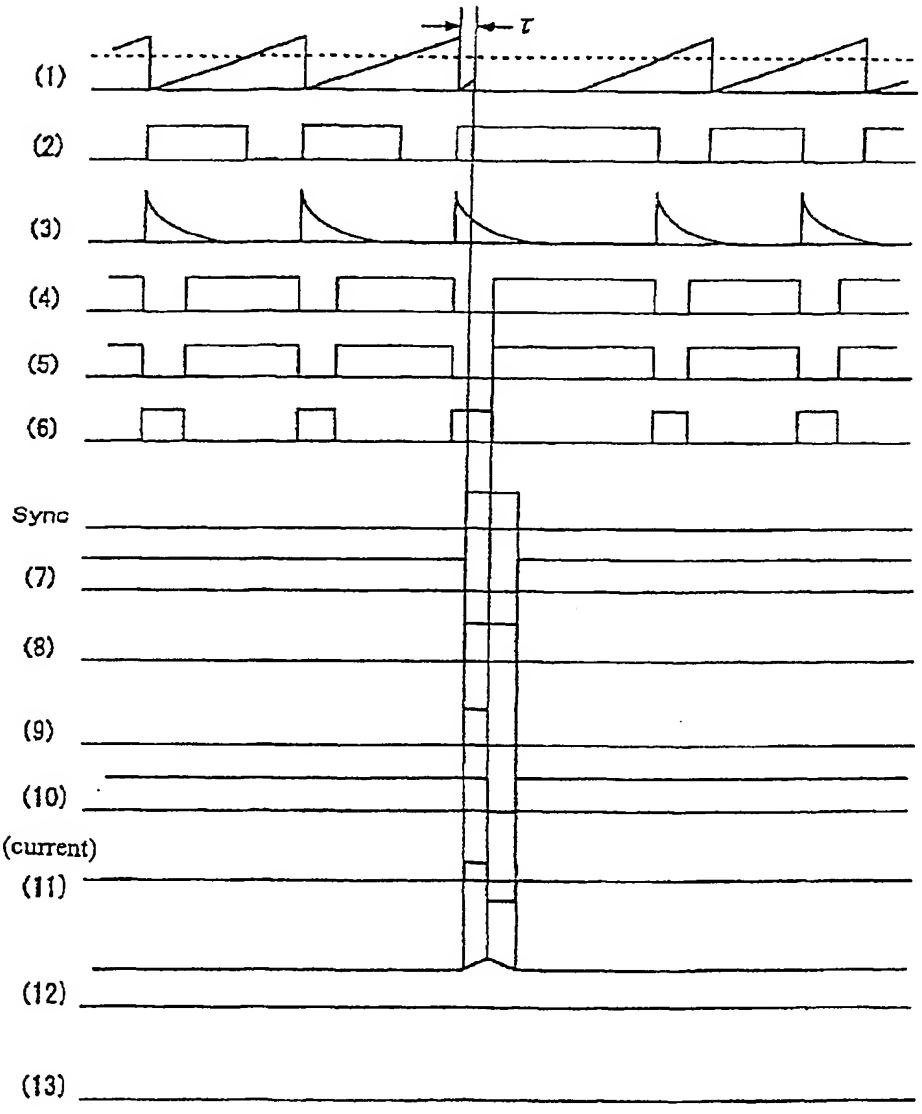


FIG. 8

Diagram showing each part of the waveform in the phase advanced state of the circuit shown in Figure 6.

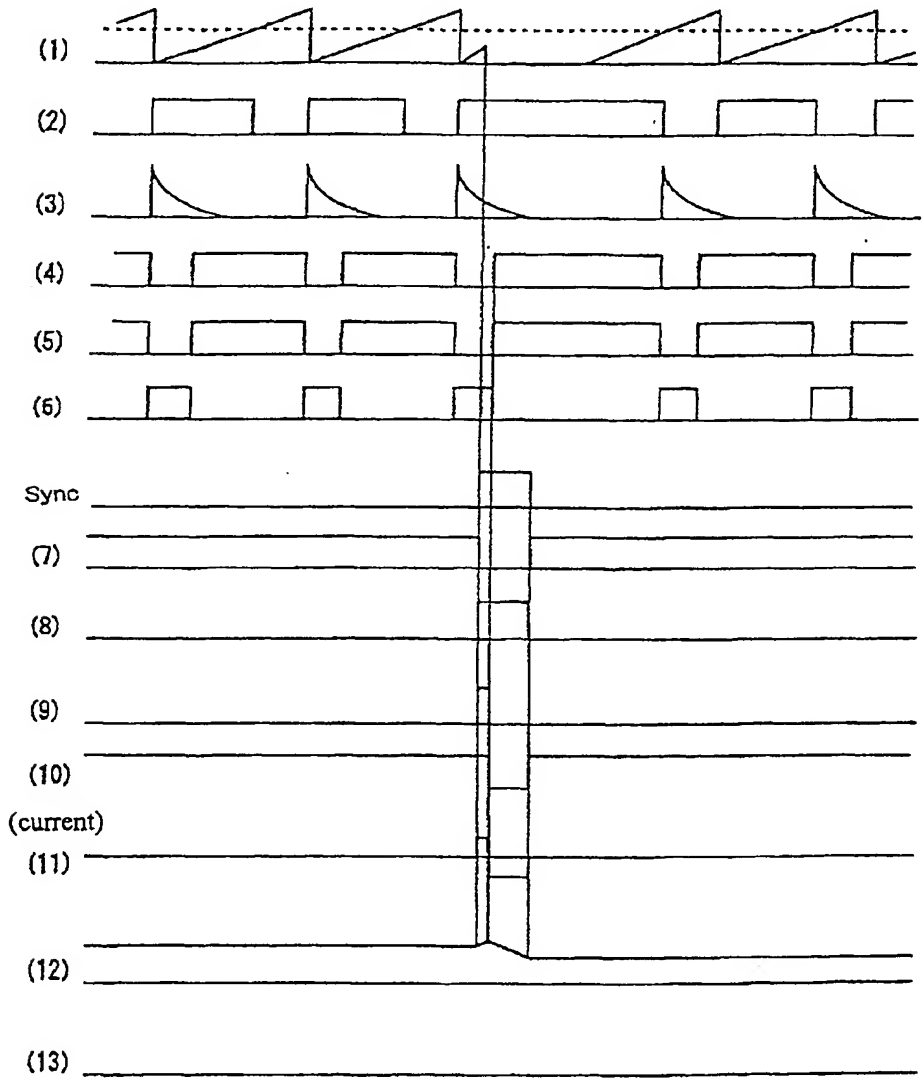


FIG. 9

Diagram showing each part of the waveform in the interrupted state of the circuit shown in Figure 6.

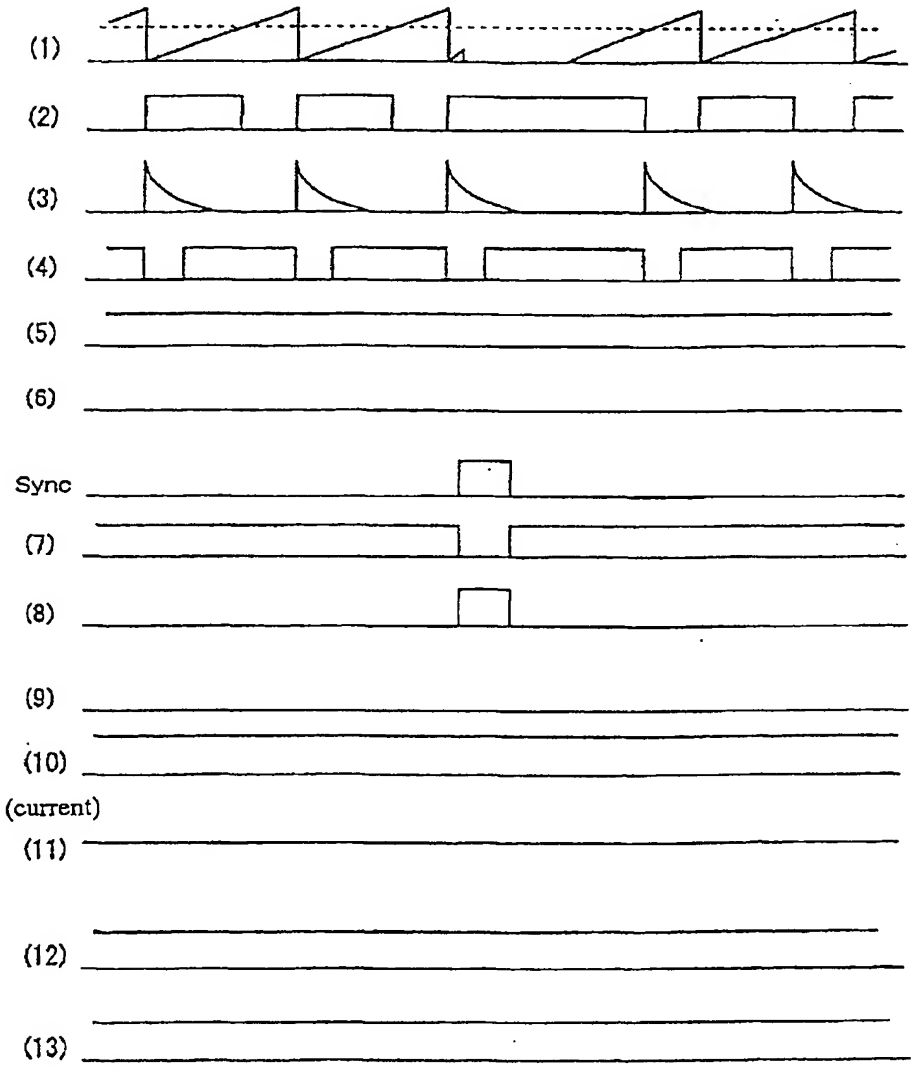


FIG. 10

Diagram showing an example of the structure of the lighting circuit of the dielectric barrier discharge fluorescent lamp using a push-pull inverter circuit.

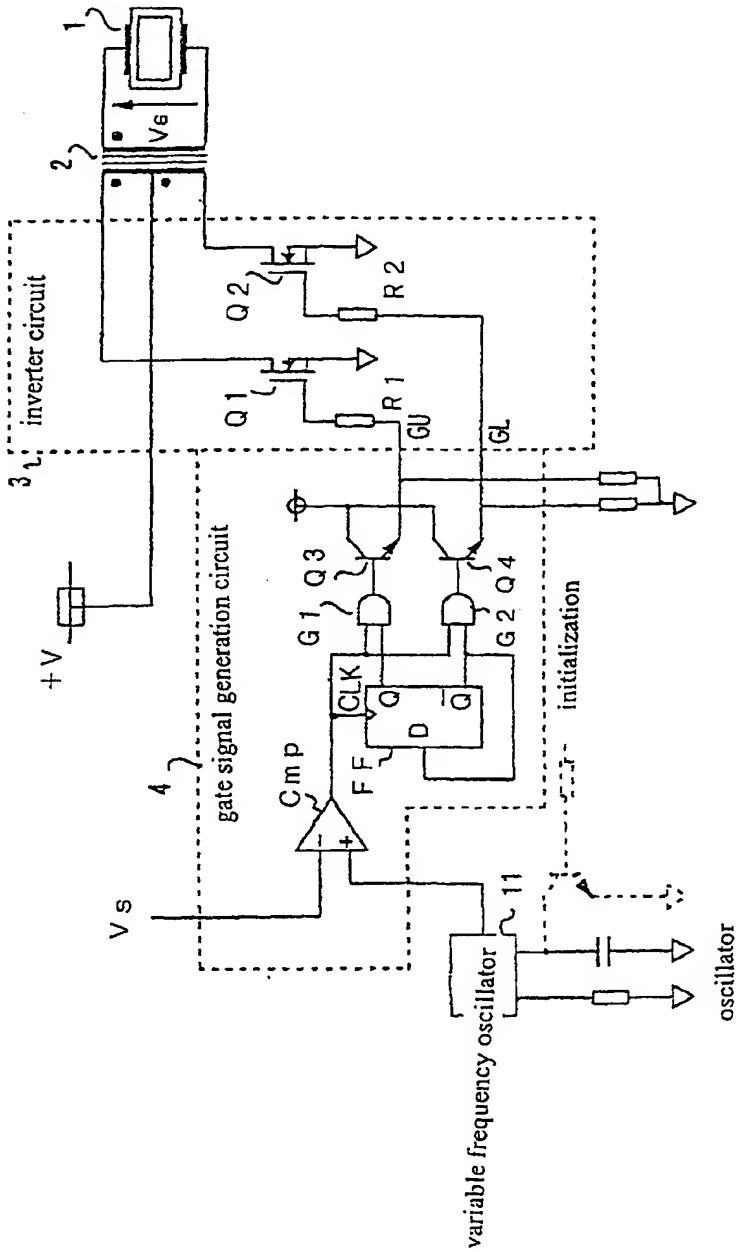


Diagram showing the operation of Figure 10.

FIG. 11(a) Vs
oscillation signal

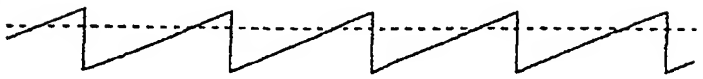


FIG. 11(b)
comparator output

FIG. 11(c)
flipflop output

FIG. 11(d)
switch device gate signal

FIG. 11(e)
switch device gate signal

FIG. 11(f)
lamp voltage

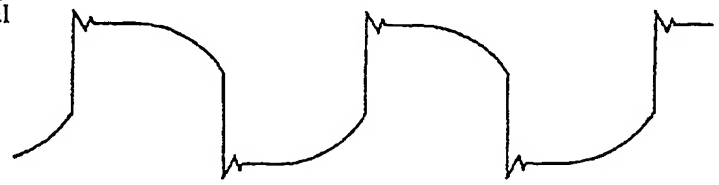


FIG. 12

Diagram explaining the state in which the external synchronization signal and the inverter oscillation phase do not overlap.

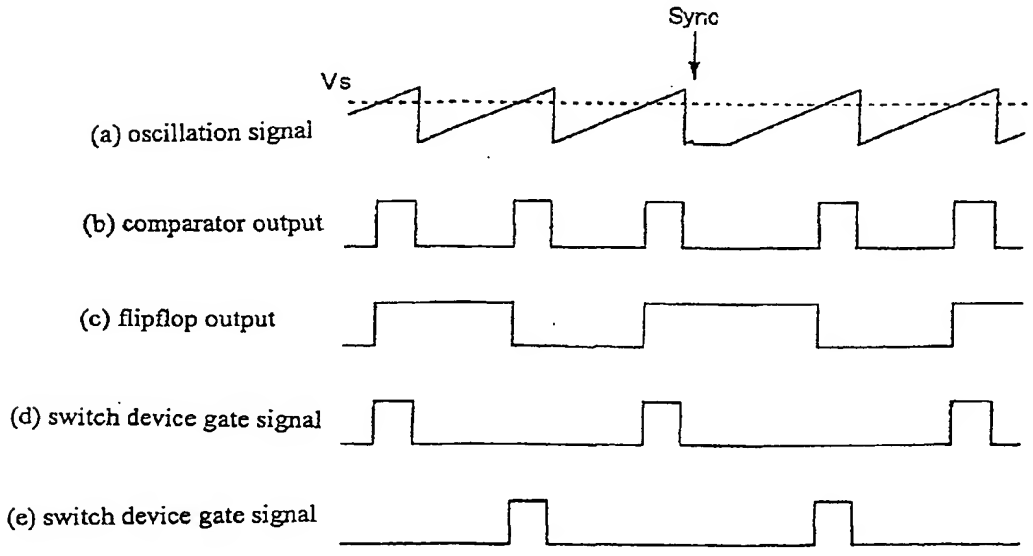


FIG. 13

Diagram explaining the state in which the external synchronization signal and the inverter oscillation phase overlap.

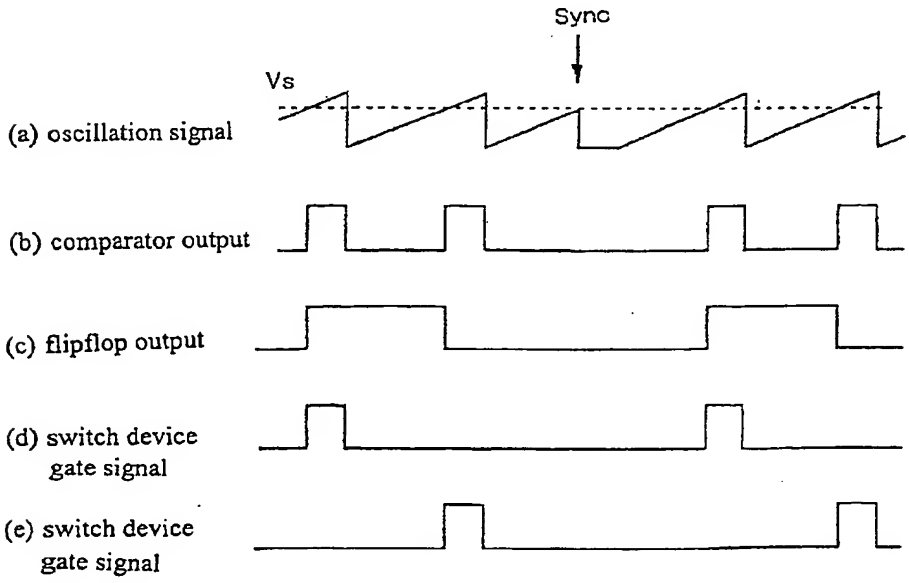
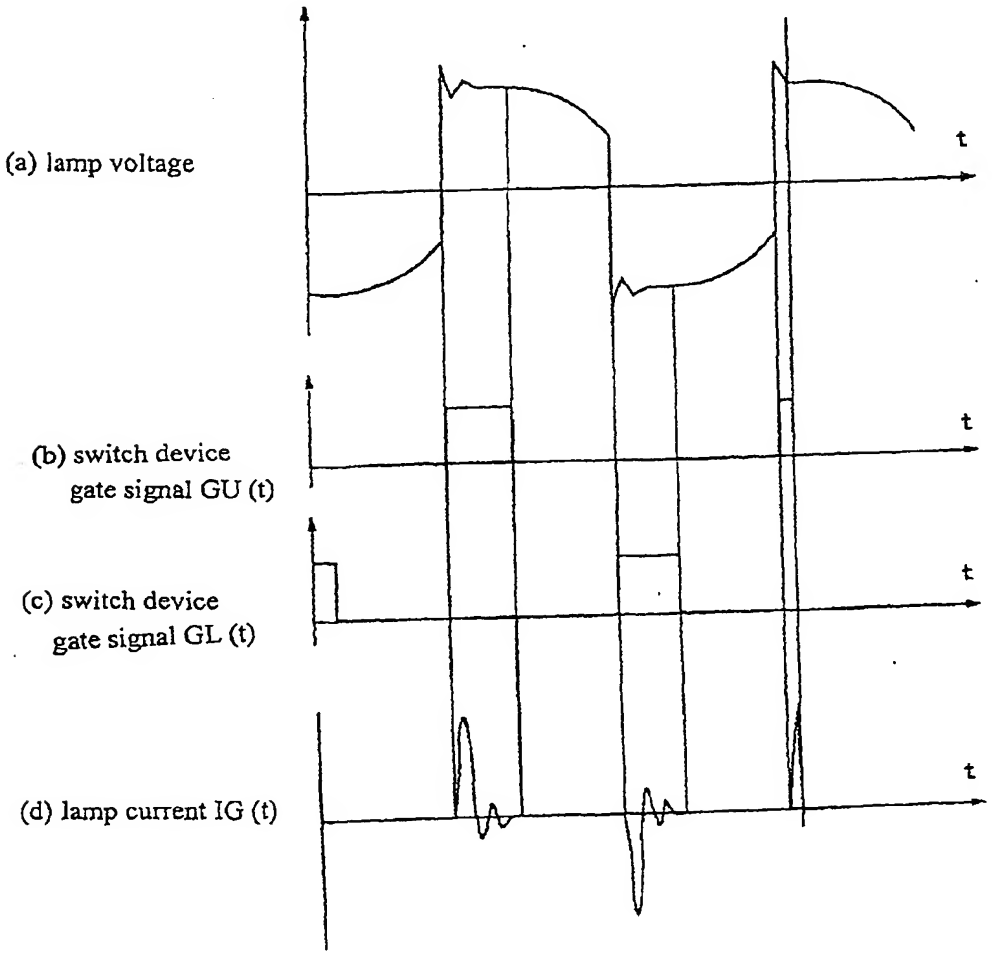


FIG. 14

Diagram showing the state in which the external synchronization signal and the inverter oscillation phase overlap when the switch device ON duration of the inverter is short.



INTERNATIONAL SEARCH REPORT

International application No.
PCT/JP00/03012

A. CLASSIFICATION OF SUBJECT MATTER
Int.Cl[7] H05B41/24

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
Int.Cl[7] H05B41/24

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
Jitsuyo Shinan Koho 1940-1996 Toroku Jitsuyo Shinan Koho 1994-2000
Kokai Jitsuyo Shinan Koho 1971-2000 Jitsuyo Shinan Toroku Koho 1996-2000

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US, 5936358, A (Ushio Denki Kabushiki Kaisha), 14 April, 1998 (14.04.98), Full text; Figs. 1 to 10 & EP, 831517, A2 & JP, 10-97898, A	1-2
A	JP, 8-31585, A (USHIO INC.), 02 February, 1996 (02.02.96), Full text; Figs. 1 to 12 (Family: none)	1-2

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Date of the actual completion of the international search	Date of mailing of the international search report
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